A SIMULATION AND EVALUATION SCHEME FOR SINGLE EVENT EFFECTS IN VLSI

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Abstract

Due to the complexity of large scale integrated circuits, it can become time consuming to analyse Single Event Effect (SEE) in large circuits. Hence, this paper proposes a rapid simulation scheme for large scale circuits. It takes advantage of transistor simulation tools and VLSI digital simulation tools to achieve both high accuracy and efficiency. The experiment results show that one million SEEs can be injected into the S27 circuit in 55 s, while the HSPICE simulation takes 67000 times longer. Index Terms—Single event effect, Fault injection, SEE model, SEE Mitigation, HDL simulation, VLSI.

Introduction

In order to mitigate Single Event Effects (SEEs), a series of simulation methods have been proposed to conduct SEE evaluation. Typically, such simulation studies include 1) transistor simulation and 2) HDL simulation. Transistor simulation tools (e.g. TCAD and SPICE) [1], [2] usually enable simulations based on currents and voltages. They are normally used for small circuits with few transistors due to the high computation effort required for larger circuits. HDL simulations are used for large scale circuits. However, error rates and propagation paths may change due to the physical layouts, which are not covered in the typical HDL simulation. In order to overcome these shortcomings, we have proposed a new scheme where the SEE models of logic gates are built in SPICE simulations and the evaluation is conducted in HDL simulations, so that it may achieve both accuracy and efficiency. In addition, it can create universal simulation environments to compare the relative SEE mitigation performance of different circuits.

The Workflow of the Proposed see Evaluation

The proposed scheme includes three parts: 1) build SEE behavior models for the employed logic gates from SPICE simulations, 2) rebuild the HDL net lists of the target circuits using digital SEE models and 3) conduct HDL simulations to analyse SEE behaviors in large scale circuits

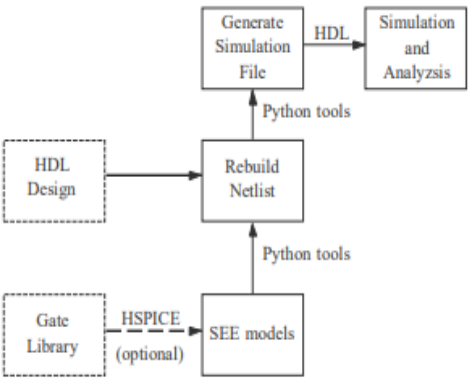

Figure 1 The Work Flow of the Proposed Scheme

The work flow of the proposed SEE simulation scheme is shown in Fig. 1. In the proposed scheme, the first step is to build SEE models by using a transistor simulation tool, which is HSPICE here. The transient currents corresponding with the radiation intensity will be injected to the sensitive node to indicate SEEs. The voltage changes at the output ports will be recorded to build SEE behavior models. The generated SEE models contain the information about pulse width, output delay and possibilities of errors. The models can be reused to reduce the simulation time of this scheme. The second step is to rebuild the net list and generate simulation files. In order to inject the SEEs in the HDL simulation, the SEE models are represented by HDL tasks, which are bound to specific logic gates. The employed logic gates in the net list will be replaced by the redesigned modules with SEE tasks. In the HDL simulation, the respective tasks will be executed to inject SEEs. In this scheme, we designed scripts tools using Python to carry out this step automatically. The final step is to conduct the simulation, analyse the results and optimise the designs. A set of SEE models can be used to create an unified simulation environment. By using the same set of SEE modules, we can quickly evaluate and compare the SEE mitigation performance of different circuits without taking weeks or months to conduct transistor level simulations.

Generation of See Models

In this paper, we introduce a novel SEE model for HDL simulations. The SEE models are a set of functions based on transistor simulations, which can be represented by the behaviors of the specific circuit modules struck by the particles. The mathematical representation of SEE models includes two parts: 1) the behaviors of the circuits without errors and 2) the behavior of the SEEs. Behaviors of SEE models are collected in SPICE simulations. In the proposed scheme, the transient currents are used to indicate SEEs. They will be injected to sensitive circuits nodes. The changes in output will be noted to analyse SEE behaviors. The SEE behavior can be represented by following parameters: 1) probability of specific outputs, when the gate is struck, 2) width of the transient pulses, 3) the hit delay, which indicates the time for pulses to show up, and 4) the propagation

effects of input pulses. In order to cover all probabilities of SEE behaviors, the input values, circuit states and injected nodes are considered in HSPICE. Considering the complexity and reusability, we use basic logic gates to build SEE models. The time required to build SEE models are shown in the Table I. For small logic gates (e.g. INVX2M), the HSPICE simulation can be done in 500 s. For complex sequential circuits (e.g. QFFQX1M), it will take 200 minutes to build SEE models.

Table 1 Time Required of the Spice Simulation to Build See Models

Unit	Size*	probabilities**	Time required
INVX2M	2	4	1 s
OR2X1M	6	24	16 s
OR3X1M	8	32	31 s
OR4X1M	10	160	238 s
NOR2X1M	4	16	6 s
NOR3X1M	6	48	32 s
NOR4X1M	8	128	121 s
AND2X1M	6	24	16 s
AND3X1M	8	32	31 s
AND4X1M	10	160	238 s
NAND2X1M	8	32	6 s
NAND3X1M	10	160	32 s
NAND4X1M	12	192	480 s
QFFQX1M	25	176	196 min

* Number of transistors inside circuits
** Number of cases, which will cause output changes

HDL Simulations of Sees in Large Circuits

In this paper, we conduct the HDL simulation using the ISCAS89 benchmark [3] circuits to verify the proposed scheme. In those circuits, the S27 circuit is the smallest, which contains 15 circuit units and the S28584 circuit is the largest, which contains 11448 circuit units. The simulation results in the circuits indicate the effects of the SET and SEU on circuits from small scale to large scale. The time cost of HDL simulation for ISCAS89 benchmark circuits is elaborated. We can evaluate the time required for the HDL simulation by averaging time costs for each SEE injection.

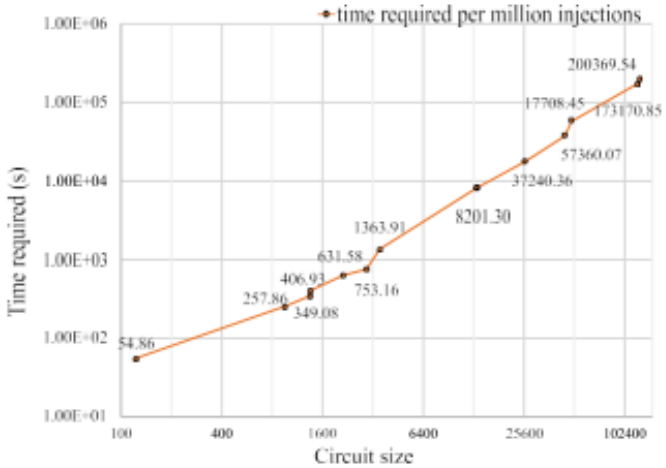

Figure 2 The Time Required to SEE HDL Simulations for ISCAS89 Benchmark Circuits

Fig.2 shows the time required for the HDL simulation with one million SEE injections in the ISCAS89circuits. By using HDL models, one million SEEs can be injected into S27 circuit (121 transistors) in just 55 s, while it will take 55 hours in S38584 (125940 transistors). The time required for SEE simulation increases nearly linearly with the scale of the circuits. The time required for HSPICE to conduct same experiment is also tested in this paper. Take S27 as example, the time required to conduct 1 ms simulation is less that 1 s in the proposed scheme, while the SPICE will take more than 67000 s. The obtained results exhibit the efficiency of the proposed scheme.

Conclusion

This paper proposed a fast SEE simulation scheme to evaluate the effects of SEE on large scale circuits. We used SPICE simulations to build a set of general SEE models to simplify the processes of the evaluation of SEE effects on large scale circuits. The results we obtained clearly demonstrate the time efficiency of the scheme.

References

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